Outline

- Background – need for JTAG
- JTAG and Boundary Scan
- Advantages
- Atmel ICE mk-II and gdb
- Real JTAG Applications
Bed of Nails fixture

- PCB testing was done using Bed of Nails in circuit testing.
Past to Future – Testing

- Miniaturization results in loss of test access

Yesterday

Today

Tomorrow
Circuit Complexity / Cost

- Increasing integration at chip level complicates controllability.

Yesterday

Today
JTAG (1149.1 Standard)

- IEEE 1149.1, a standard 5-pin serial protocol that established the details of access to any chip with JTAG port.

- Features:
  - Boundary scan testing of ICs
  - Debug Embedded devices
  - System level debug capability
Boundary scan is a methodology allowing complete controllability and observability of the boundary pins of a JTAG compatible device via software control.
Boundary Scan Principle

The top level schematic of test logic defined by IEEE Std 1149.1 includes three key blocks:

- **The TAP Controller**
  - This responds to the control sequences supplied through the test access port (TAP) and generates the clock and control signals required for correct operation of the circuit blocks.

- **The Instruction Register**
  - This shift register-based circuit is serially loaded with the instructions that selects an operation to be performed.

- **The Data Registers**
  - These are a bank of shift register based circuits. The stimuli required by an operation are serially loaded into the data registers selected by the current instruction. Following execution of the operation, results can be shifted out for examination.
What can it be used for

- The standard defines instructions that can be used to perform
  - Functional Tests
  - Interconnect Tests
  - Built-in self test procedures
Advantages

- Need for physical test points on board is eliminated => simpler board layouts
- Cheap test fixtures
- Reduced time on in-circuit test systems
- Increased use of standard interfaces
- Faster time-to-market
Widespread uses

- A large proportion of high end embedded systems have a JTAG port.
- The PCI bus connector standard contains optional JTAG signals (pins 1-5); PCI-Express contains JTAG signals (pins 5-9). A special JTAG card can be used to re-flash a corrupt BIOS.
- Almost all FPGAs and CPLDs used today can be programmed via the JTAG port.
JTAG Software

- **Open Source**
  - UrJTAG project supports many JTAG tools, processors, and boards.
  - OpenOCD project supports various inexpensive JTAG adapters including USB ones based on FT2232 chips, and is mostly used with ARM projects. It provides GDB and telnet interfaces, both from Linux and from MS-Windows.

- **Freeware**
  - Atmel provides AVR Studio on MS-Windows, for AVR8 microcontrollers, and a cross-platform AVR32studio product to support AVR32 systems.
  - Xilinx provides lower end FPGA development tools at no cost.
  - HappyJTAG2 is embedded JTAG solution with FT2232 chip for AVR8 microcontrollers and Atmel AVR Studio on MS-Windows.
Working

Source: http://www.corelis.com/products/ScanExpressJET.htm
JTAG ICE mkII and gdb.

- **Functions** -
  - Run
  - Stop
  - Step
  - Write to Registers and memory
  - Read from Registers and memory
  - Exchange parameters with the JTAG host
  - Display CPU status

Refer: http://www.youtube.com/watch?v=lwPWq9m0M6w
Real applications

- Design Verification/Debug
  - Provides control and observation of system under test without need for physical access

- Manufacturing Test
  - Provides test and diagnostic capabilities of in-circuit test without need/expense of physical access

- System Configuration Maintenance
References

- http://www.embedded.com/story/OEG20021028S0049
- http://www.corelis.com/products/ScanExpressJET.htm
Thankyou 😊
Extra Slides
Test Access Ports

- The JTAG Test Access Port (TAP) contains four pins that drive the circuit blocks and control the operations specified. The TAP facilitates the serial loading and unloading of instructions and data.

- Four pins of TAP are:
  - TMS – Test mode Select
  - TCK – Test Clock
  - TDI – Test Data Input
  - TDO – Test Data Output
The function of each TAP pin is as follows:

- **TCK** - this pin is the JTAG test clock. It sequences the TAP controller as well as all of the JTAG registers.

- **TMS** – this pin is the mode input signal to the TAP Controller. The state of TMS at the rising edge of TCK determines the sequence of states for the TAP controller.

- **TDI** – this pin is the serial data input to all JTAG instruction and data registers. TDI is sampled into the JTAG registers on the rising edge of TCK.

- **TDO** - this pin is serial data output for all JTAG instruction and data registers. TDO changes state on the falling edge of TCK and only active during shifting of data through device. This pin is three-stated at all times.
SECON S JTAG TESTER

Source: http://www.jtagtest.com/images/jtagtest_linux.png